Remarks/Arguments

The Office Action mailed on May 28, 2008 has been reviewed and carefully considered.

Claims 1-12 and 14-21 are now pending in this application. Claim 13 remains canceled without prejudice. Reconsideration of the above-identified application, in view of the following Remarks, is respectfully requested.

Rejections under 35 U.S.C. §103(a)

Claims 1-4, 6-7, 9-12 and 15-21 currently stand rejected under 35 U.S.C. §103(a) in view of U.S. Patent Publication 2004/0205158 (hereinafter 'Hsu'), purportedly admitted prior art (hereinafter 'PAPA'), "Clock Solutions for WiFi (IEEE 802.11)" by Brandon Ogilvie (hereinafter 'Ogilvie') and U.S. Patent No. 7,110,783 to Bahl et al. (hereinafter 'Bahl'). Applicant respectfully requests reconsideration of the Examiner's §103(a) rejection in light of the following comments.

Claim 1 of the present application recites:

"A method, comprising:

'scanning, by a wireless local area network scanner in a wireless device, to detect the presence of a wireless local area network WLAN;

'detecting the presence of said wireless local area network by employing said wireless local area network scanner to identify energy fluctuations without a wireless local area network baseband circuit being activated to process data;

'contacting a base station of said wireless local area network by the wireless local area network baseband circuit in said wireless device in response to detection of said wireless local area network to request location of said base station; and

'receiving location of said wireless local area network."

As discussed in the responses to the Office Actions dated September 20, 2007 and December 26, 2007, Hsu discloses a wireless device that utilizes a tuner to scan for a WLAN beacon (see, e.g. Hsu, paragraphs 64, 78). However, Hsu fails to discuss any specific details whatsoever regarding how the beacon is detected. Accordingly, Hsu does not disclose or

render obvious the feature of detecting the presence of a WLAN by identifying energy fluctuations without a WLAN baseband circuit being activated to process data.

In support of the rejection of claim 1, the Examiner states that PAPA indicates that it is well-known to one of ordinary skill in the art that a WLAN baseband circuitry need not be activated to detect the presence of a WLAN. Specifically, the Examiner cites the following portion of the Applicant's Specification in support of the assertion:

> "The frequency reference accuracy specified in WLAN standards (e.g., .+-.25 ppm as specified in the IEEE 802.11b standard) can allow the PLL circuit 314 to operate without automatic frequency control (AFC) provided by the WLAN baseband circuitry. As such, the WLAN baseband circuitry 208 does not have to be activated to detect the presence of the WLAN, thereby conserving power and saving battery life in the mobile device."

(Specification, p. 10, lines 15-18)

However, as discussed in the response to the office action dated December 26, 2007, regarding known prior art, PAPA simply indicates that standard frequency reference accuracies themselves are known ('+-.25 ppm as specified in the IEEE 802.11b standard'). PAPA does not state that operating a PLL without automatic frequency control is well known in the art. Therefore, the description in the Specification concerning PLL circuit operation without AFC cannot be relied upon in the rejection of claim 1. See MPEP 2141 (stating that patentability must be assessed 'at the time the invention was made' to avoid impermissible hindsight) (citing W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)). See also MPEP 2142 (stating that '[k]nowledge of applicant's disclosure must be put aside' in determining obviousness).

To support the assertion that "the frequency reference accuracy specified in WLAN standards (e.g., .+-.25 ppm as specified in the IEEE 802.11b standard) can allow the PLL circuit 314 to operate without automatic frequency control (AFC) provided by the WLAN baseband circuitry" is well-known in the art, the Examiner cites Ogilvie and, purportedly, Bahl. While Ogilvie does not support the assertion that such features are well known in the art, for expediency purposes, the Applicant notes that Ogilvie is not a prior art reference. The priority date of the current application is August 22, 2003, the date on which the current application was first filed in accordance with the Patent Cooperation Treaty. The date of

Ogilvie is September 3, 2003, as provided in the margin at the bottom of page 1 of Ogilvie according to the American convention of month/day/year. As evidence that the American convention was used in the Ogilvie reference, submitted herewith is another reference from the same "Application Notes" series as Ogilvie, provided by Pericom, entitled, "DDR2: The Next Generation Main Memory" by Jimmy Ma, retrieved from http://www.pericom.com/applications/an_listall.php, which also lists the Ogilvie reference. The Ma reference is dated "08/18/04," clearly indicating that the Application Notes series employs the American dating convention. Accordingly Ogilvie may not be utilized to demonstrate what features were known in the art at least because it is not a prior art reference. Thus, Ogilvie, taken singly or in combination with any other art of record, does not render claim 1 obvious.

With regard to Bahl, firstly, Bahl does not in any way demonstrate that "the frequency reference accuracy specified in WLAN standards (e.g., .+-.25 ppm as specified in the IEEE 802.11b standard) can allow the PLL circuit 314 to operate without automatic frequency control (AFC) provided by the WLAN baseband circuitry" is well-known in the art. Bahl simply states that a separate, low-power transceiver should be employed to exchange channel scheduling information on a low power channel in lieu of a high power receiver that utilizes a high power channel (see, e.g., Bahl, column 6, lines 48-61; column 9, lines 4-13). Nowhere does Bahl disclose that "the frequency reference accuracy specified in WLAN standards (e.g., .+-.25 ppm as specified in the IEEE 802.11b standard) can allow the PLL circuit 314 to operate without automatic frequency control (AFC) provided by the WLAN baseband circuitry."

Secondly, Bahl also fails to disclose or render obvious the feature of detecting the presence of a WLAN by identifying energy fluctuations without a WLAN baseband circuit being activated to process data. Although Bahl discloses employing the low-power transceiver to detect detection signals transmitted by a host transceiver (see, e.g., Bahl, column 8, lines 28-41), Bahl does not disclose any details whatsoever concerning how the detection is performed in the low-power transceiver. Thus, Bahl fails to teach or remotely suggest the feature of detecting the presence of a WLAN by identifying energy fluctuations without a WLAN baseband circuit being activated to process data.

Furthermore, it should be noted that even if it were well known in the art that it is possible to run a PLL circuit without automatic frequency control, the Examiner has not

identified any means in the prior art for detecting the presence of a WLAN by identifying energy fluctuations without processing signals for data or without performing carrier recovery. Thus, even if it were known that a PLL circuit may run without automatic frequency control, one of ordinary skill in the art could not recognize how to implement such a feature to detect the presence of a WLAN. In contrast, in accordance with one or more implementations described in the Specification, a means for detecting a WLAN by identifying energy fluctuations without processing data and without performing carrier recovery has been developed (see, e.g. Specification, p. 9, line 1 to p. 10, line 11; p. 11, lines 10-23). Accordingly, claim 1 is believed to be patentable over Hsu, PAPA and Bahl, taken singly or in combination, at least because the references fail to disclose or render obvious at least the feature of detecting the presence of a WLAN by identifying energy fluctuations without a WLAN baseband circuit being activated to process data. Moreover, claims 2-4, 6, 7 are believed to be patentable over Hsu in view of PAPA and Bahl due at least to their dependencies from claim 1.

With regard to the patentability of claim 9, claim 9 recites, inter alia:

> "detecting the presence of said wireless local area network by identifying energy fluctuations of a wireless local area network signal without performing carrier recovery to detect the presence of said wireless local area network."

As discussed above, Hsu and Bahl do not provide any specific details concerning how WLAN beacons or detection signals are detected. Accordingly, Hsu and Bahl, taken singly or in combination, do not disclose or remotely suggest detecting the presence of a WLAN by identifying energy fluctuations without performing carrier recovery. Furthermore, as discussed above, PAPA and Ogilvie may not be relied upon to render claim 9 obvious. Thus, claim 9 is believed to be patentable. Moreover, claims 10-12 and 15 are also believed to be patentable due at least to their dependencies from claim 9.

In addition, claim 16 is not obvious over Hsu, PAPA, Ogilvie and Bahl, as claim 16 includes similar features discussed above regarding claim 1. Claim 16 recites, inter alia:

"detecting the presence of said wireless local area network by employing said wireless local area network scanner to identify energy fluctuations without a wireless local area network baseband circuit being activated to process data."

Thus, claim 16 is believed to be patentable for at least the reasons discussed above with regard to claim 1. Claims 17-21 are also believed to be patentable due at least to their dependencies from claim 16.

As such, withdrawal of the rejection is respectfully requested.

Claim 5 currently stands rejected under §103(a) in view of Hsu, PAPA, Ogilvie and Bahl in further view of United Stated States Patent Application Publication No. 2004/0264395 (hereinafter 'Rao'). Applicant respectfully requests reconsideration of the Examiner's §103(a) rejection in light of the following comments.

Claim 5 is dependent from claim 1 and thus also includes, inter alia, the feature of "detecting the presence of said wireless local area network by employing said wireless local area network scanner to identify energy fluctuations without a wireless local area network baseband circuit being activated to process data." As discussed above, Hsu and Bahl do not disclose or render obvious at least this feature. Furthermore, as discussed above, PAPA and Ogilvie cannot be relied upon in rejecting claims of the present application.

In addition, Rao does not disclose or render obvious the above-recited feature of claim 5. Rao is directed to methods and apparatuses for automatically configuring a wireless network client by identifying wireless local network access points upon detecting a wireless local network message (see, e.g., Rao, paragraph 8). However, Rao merely states that WLAN access points are discovered and a broadcast message is detected by the wireless client (see, e.g., Rao, paragraphs 43 and 53). No specific details concerning how the WLAN access points are detected are provided by Rao in any way. Moreover, the reference certainly does not disclose or remotely suggest that a baseband circuit is deactivated while identifying a WLAN broadcast message to detect the presence of a wireless network.

Accordingly, claim 5 is believed to be in condition for allowance at least because Rao, Hsu and Bahl, taken singly or in combination, fail to disclose or render obvious the feature of

detecting the presence of a wireless local area network by identifying energy fluctuations without a wireless local area network baseband circuit being activated to process data.

Claims 8 and 14 currently stand rejected under 35 U.S.C. §103(a) in view of Hsu, PAPA, Ogilvie, Bahl and in further view of United States Patent Application Publication No. 2003/0134650 (hereinafter 'Sundar'). Applicant respectfully requests reconsideration of the Examiner's §103(a) rejection in light of the following comments.

Claim 8 is dependent on claim 1 and includes, inter alia, the feature of "detecting the presence of said wireless local area network by employing said wireless local area network scanner to identify energy fluctuations without a wireless local area network baseband circuit being activated to process data," as described above. In addition, claim 14 is dependent on claim 9 and thereby includes, inter alia, "detecting the presence of said wireless local area network by identifying energy fluctuations of a wireless local area network signal without performing carrier recovery to detect the presence of said wireless local area network."

As discussed more fully in the responses to the Office Actions dated September 20, 2007 and December 26, 2007, Sundar does not disclose or render obvious the feature of identifying energy fluctuations without performing carrier recovery to detect the presence of a wireless LAN. Firstly, Sundar merely discloses inferring the presence of a wireless LAN by detecting RF energy in the permitted frequency range (see, e.g., Sundar, paragraphs 55-58). Sundar does not disclose or remotely suggest identifying energy fluctuations to detect the presence of a wireless LAN. Secondly, Sundar also fails to disclose detecting the presence of a WLAN without a wireless local area network baseband circuit being activated to process data. Rather, Sundar discloses processing a beacon frame to obtain an SSID, comparing the SSID to a list of SSIDs and if there is a match, inferring the presence of a valid WLAN (see, e.g., Sundar, paragraph 55-58). Extraction of an SSID necessarily entails the activation of a WLAN baseband circuit to process data. Thus, Sundar fails to disclose or remotely render obvious detecting the presence of a WLAN without a wireless local area network baseband circuit being activated to process data. Similarly, Sundar also fails to disclose or render obvious the claim 14 feature of detecting the presence of a WLAN without performing carrier recovery, as carrier recovery is performed to extract data from a WLAN carrier signal.

Accordingly, Sundar fails to disclose or render obvious the feature of "detecting the presence of said wireless local area network by employing said wireless local area network scanner to identify energy fluctuations without a wireless local area network baseband circuit being activated to process data" and the feature of "detecting the presence of said wireless local area network by identifying energy fluctuations of a wireless local area network signal without performing carrier recovery to detect the presence of said wireless local area network," as included in claims 9 and 14, respectively. In addition, as discussed above, Hsu and Bahl also fail to disclose or render obvious these features of claims 9 and 14. Moreover, as discussed above, PAPA and Ogilvie cannot be relied upon in rejecting claims of the present application. Thus, claims 9 and 14 are believed to patentable for at least the reasons stated. Withdrawal of the rejection is respectfully requested.

Finality of the Rejection

It is respectfully submitted that the finality of the Office Action dated May 28, 2008 is improper, as the Examiner has asserted a new ground of rejection that was not necessitated by amendment or submission of an information disclosure statement.

MPEP § 706.07(a).

> Under present practice, second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims, nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p).

The grounds of the rejection of claim 1, set forth in the preceding Office Action dated December 26, 2007, were based upon Hsu in view of purportedly well known and admitted prior art. In the Final Office Action, the Examiner has cited an additional reference, Bahl, substantively in the rejection of claim 1 (see, e.g., Office Action dated May 28, 2008, p. 10). The Examiner alleges that Bahl was cited to show that "the frequency reference accuracy specified in WLAN standards (e.g., .+-.25 ppm as specified in the IEEE 802.11b standard) can allow the PLL circuit 314 to operate without automatic frequency control (AFC) provided by the WLAN baseband circuitry," as described in the Applicant's Specification, is well known in the art (see, e.g., Office Action dated May 28, 2008, p. 10). However, Bahl

nowhere discusses PLL circuits or automatic frequency control in any way. Rather, the Examiner cites Bahl to purport that "identifying energy fluctuations without a wireless baseband circuit being activated to process data" was disclosed in Bahl (Office Action dated May 28, 2008, p. 20, lines 13-14). Thus, the Examiner has asserted a new ground of rejection of claim 1.

Furthermore, the Applicant has not amended claim 1 nor has submitted the newly relied upon reference in an information disclosure statement. Accordingly, because the Examiner has asserted a new ground of rejection of claim 1 that was not necessitated by amendment or submission of an information disclosure statement, the finality of the rejection is improper (see also MPEP § 2144.03(D) ("If the newly cited reference is added for reasons other than to support the prior common knowledge statement and a new ground of rejection is introduced by the examiner that is not necessitated by Applicant's amendment of the claims, the rejection may not be made final.") (emphasis added)). As such, withdrawal of the finality of the rejection is respectfully requested.

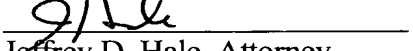
Conclusion

In view of the foregoing, Applicant respectfully requests that the rejections of the claims set forth in the Final Office Action of dated May 28, 2008 be withdrawn, that pending claims 1-12 and 14-21 be allowed, and that the case proceed to early issuance of Letters Patent in due course.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to Applicant's representatives Deposit Account No. 07-0832.

Respectfully submitted,

LOUIS ROBERT LITWIN

By: 

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August 6, 2008

DDR2: The Next Generation Main Memory

By Jimmy Ma

Introduction

Today's memory architecture shows significant improvements when compared to the days of Fast Page Mode (FPM) and Extended Data Out (EDO). The industry has shifted gear from an asynchronous world of FPM and EDO to a synchronous one. The majority of memory makers now use Synchronous Dynamic Random Access Memory (SDRAM). What was once only considered as an interim technology, SDRAM has made a significant impact on the computing market.

The first generation of synchronous memory (PC66) uses single-ended technology. And it didn't take long before PC100 and PC133 debuted with an increase in operating frequency ranging from 66MHz to 100MHz and 133MHz for PC100 and PC133, respectively. PC100 and PC133 retained the single-ended technology used in PC66. But as demands for higher speed and lower power consumption became more demanding, single-ended signaling began to reach its limitations. Once again, the memory industries have shifted gear to meet the new demand and a newer technology emerged with promises of lower power consumption and faster operating frequency. It was DDR.

DDR is an acronym for Double Data Rate, a memory technology that has evolved from its predecessor, the single-ended data rate PC100 and PC133. Double Date Rate, as its name suggests, uses technology of acquiring data on both the rising and falling edge of the clock. The technology has been well adopted in the computing and consumer markets such as workstation, desktop PC, video cards, and set-top-boxes. But with the computing and consumer markets continuing to evolve and processor speeds continuing to rise, DDR is migrating to the next generation of memory architecture to support the performance challenge. This next generation of memory is DDR2. Being the next generation of high performance memory solution, DDR2 boasts an initial clock speed of 400MHz with a data transfer rate of 3.2Gbit/s. When compared to PC100, DDR2 initial speeds have quadrupled the data rate.

Table 1 provides an overview of the performance characteristics of past and future of memory technologies. Table 2 provides a more detail overview of past and future of memory technologies:

Table 1. Memory Technology Past and Future

DRAM	Voltage	System	DIMM	Clock Frequency	Data Rate
SDR	3.3V	PC100	N/A	100MHz	0.8Gb/s
SDR	3.3V	PC133	N/A	133MHz	1.06Gb/s
DDR	2.5V	PC1600	DDR200	100MHz	1.6Gb/s
DDR	2.5V	PC2100	DDR266	133MHz	2.1Gb/s
DDR	2.5V	PC2700	DDR333	166MHz	2.7Gb/s
DDR*	2.5V	PC3200	DDR400	200MHz	3.2Gb/s
DDR-II	1.8V	PC23200	DDR2-400	200MHz	3.2Gb/s
DDR-II	1.8V	PC24300	DDR2-533	266MHz	4.3Gb/s
DDR-II	1.8V	PC25300	DDR2-667	333MHz	5.3Gb/s

Note: * = Proposed, but not yet approved by JEDEC
SDR = Single Data Rate
DDR = Double Data Rate

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Table 2. Electrical and Physical Comparison for Memory Technology Past and Future			
	PC100/133	DDR1	DDR2
Clock Frequency	100 / 133	100 / 133 / 166 / 200	200 / 266 / 333
Data Rate	100 / 133	200 / 266 / 333 / 400	400 / 533 /667
Voltage	3.3V	2.5V	1.8V
Densities	32MB – 512MB	128MB – 2GB	256MB – 4GB
Internal Banks	4	4	4 to 8
Termination for PLL in Registered DIMM	Series Termination	120	120
Type of Signaling	LVTTL	SSTL_2	SSTL_1.8
Data Strobes	Single-Ended	Differential	Single-ended or Differential
Memory Bus Width	64 Bit	64 – Bit	64 - Bit
Signal Type	Single-ended	Differential	Differential
Module Pin Count	100-Pin Unbuffered DIMM 168-Pin Registered DIMM 168-Pin Unbuffered DIMM 144-Pin SODIMM	100-Pin Unbuffered DIMM 184-Pin Registered DIMM 184-Pin Unbuffered DIMM 172-Pin MicroDIMM	240-Pin Registered DIMM 240-Pin Unbuffered DIMM 200-Pin SODIMM
Package	TSOP, FBGA, VFBGA	TSOP, FBGA	FBGA

What's new with DDR2?

Being the next generation of memory solution, the DDR2 architecture implemented multiple features to distinguish itself from DDR1. The first and most obvious feature is higher operating frequency while operating at lower supply voltage. With an initial clock speed of 400MHz, it continued where DDR1 has left off. With that, DDR2 promises to increase clock speeds up to 667MHz which means transfer rates will increase to a whopping 5.3Gb/s. This is an enormous leap from PC100 with a transfer rate of only 0.8Gb/s. Amazingly the core frequency still remains at 100MHz. The I/O buffer in PC100/133 and DDR1 are synchronous with the core with the exception that the protocol varies. In the case of DDR2, the I/O buffers are clocked twice the rate of the core frequency. What this means is DDR1 prefetches 2 bits while DDR2 is required to prefetch four bits. Figure 1 shows a graphical view of the core and I/O frequency for SDR, DDR1, and DDR2.

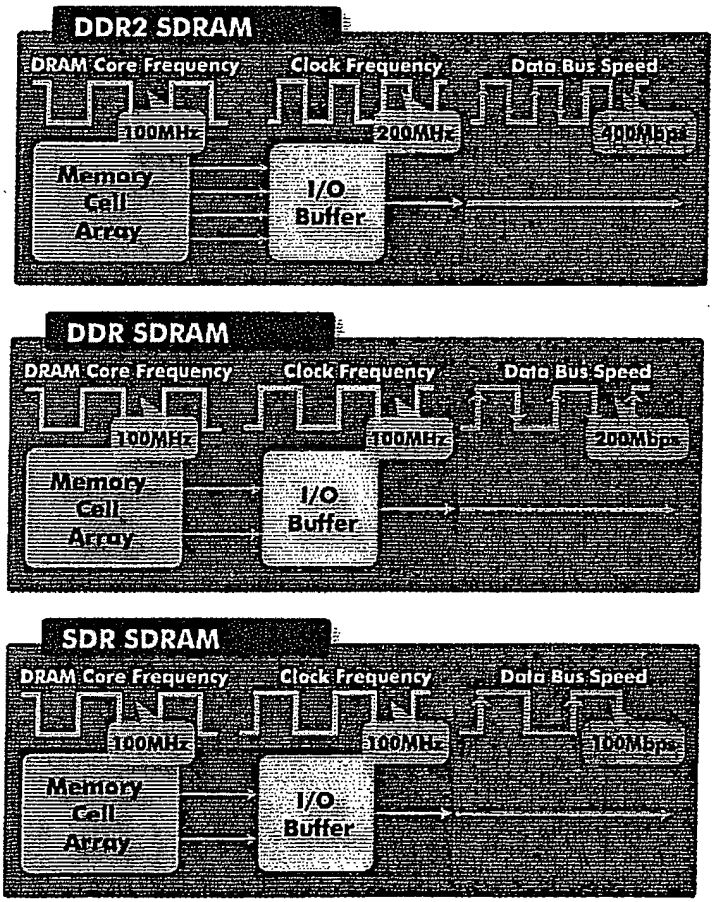


Figure 1. Memory core frequency

A Closer Look at Registered DIMM

Similar to its predecessor, DDR2 comes in both unbuffered and registered (buffered) types of DIMM (Dual Inline Memory Module). Unbuffered DIMMs are mainly used in PC desktops and notebooks, whereas, registered DIMM are mainstream in high-end platforms such as severs, datacom and telecom systems. But as system design becomes more demanding, registered DIMM may one day emerge onto the consumer desktop and notebook PCs. A complete block diagram of how a registered DIMM operates in a server is shown in Figure 3.

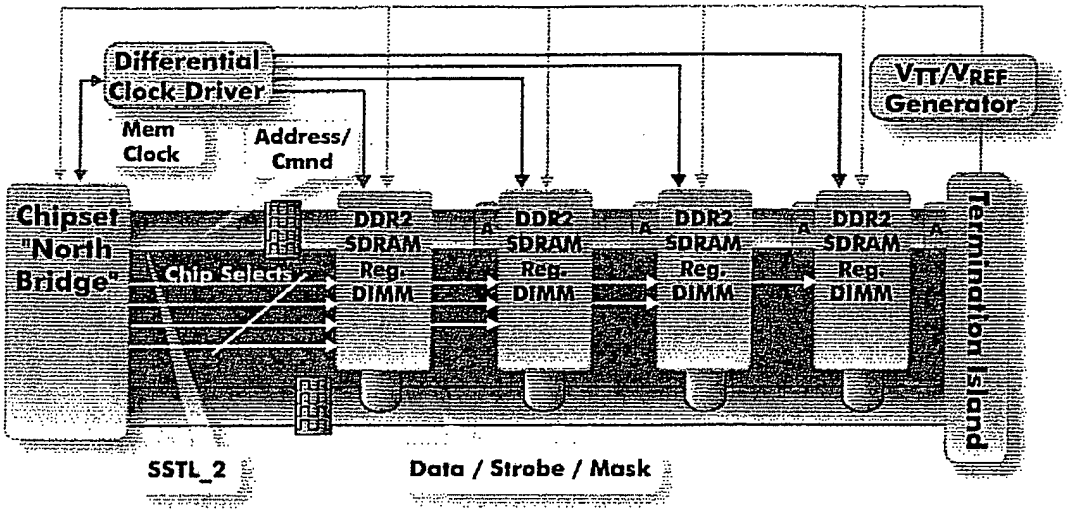


Figure 3. Overall block for a Registered DIMM

An unbuffered DIMM and a registered DIMM are somewhat similar. However, a closer look at a registered DIMM shows that there are typically three additional components: a Phase-Lock Loop (PLL) zero-delay clock buffer and two registers for a double-sided DIMM, or one register for a single-sided DIMM. The mainstream DIMM modules are double-sided DIMMs. Double-sided DIMMs have memory chips populated on both sides of the module. As mentioned earlier, registered DIMMs have a PLL. The PLL is necessary in order to distribute additional clock signals while removing any delay generated by the device itself and the traces, hence the name zero-delay buffer. A more technical explanation on how PLL generates a zero delay is provided below. The other two components, the registers, are used for address lines and control signals. The on-board registers on buffered DIMMs help reduce the system's loading caused by the DIMMs on the server board. As a result, this will allow the system to load larger capacity DIMMs and increase the number of DIMMs to be populated onto the server board. In other words, registered DIMM offers reduced system loading by allowing the MCH (Memory Controller Hub) to see it as a single load. Figure 4 is focused on the PLL and registers connection.

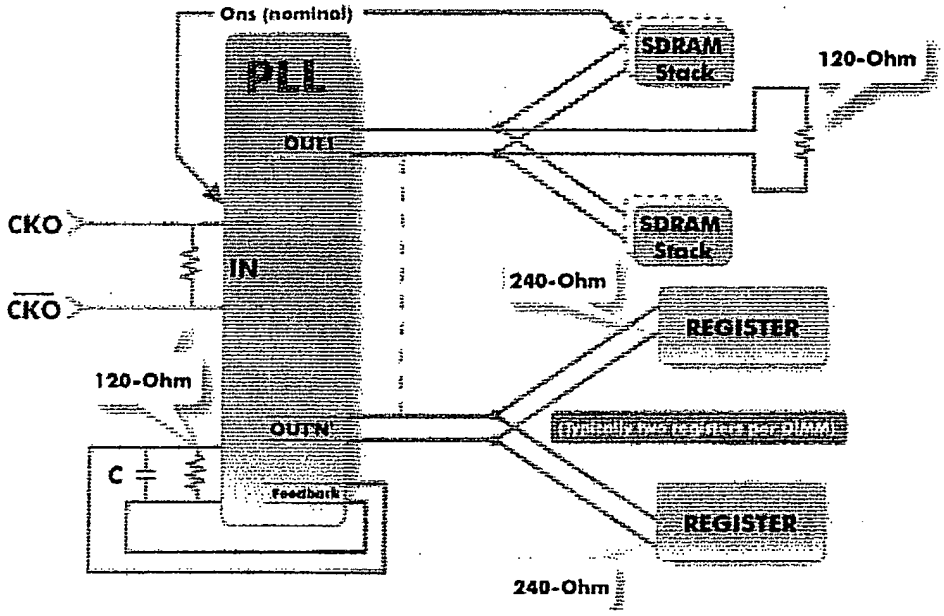


Figure 4. Architecture structure of a registered DIMM

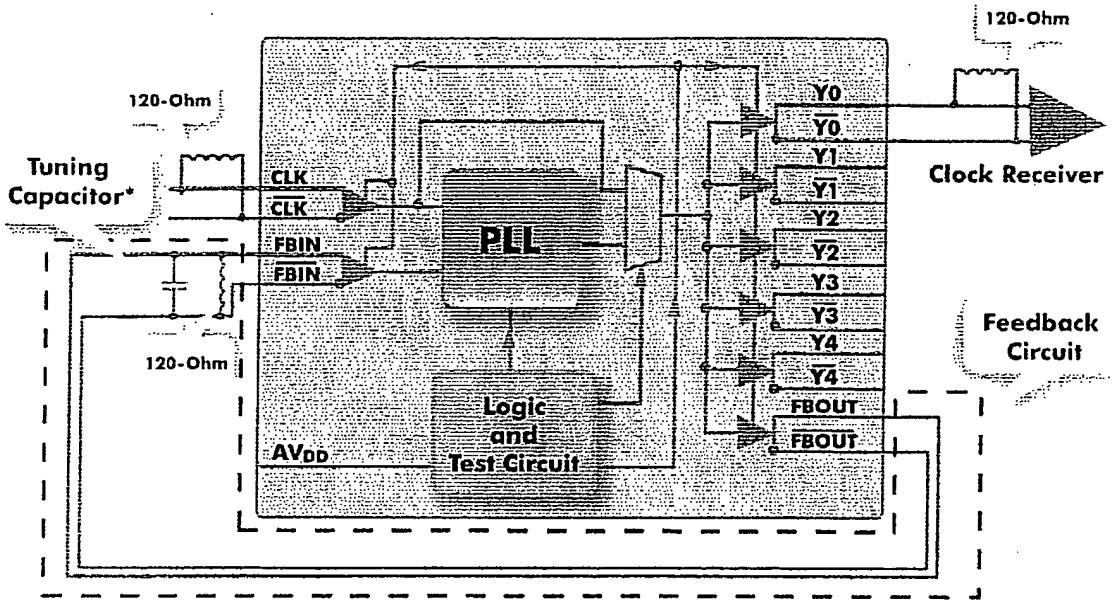
Tuning for Perfect Time

As frequencies increase, the period of each cycle becomes shorter leaving little room for any error. However, with the addition of a PLL, it provides the ability to make adjustments on the stringent timing requirement to increase the system-timing margin. The main characteristic of a PLL clock buffer compared to its counterpart, a non-PLL clock buffer, is the ability to adjust the system clock timing by altering the delay in the feedback loop.

The concept of a zero-delay buffer allows the timing between the input clock, CLK_IN signals, and the output of the clock at the destination of the memory chip, MEM_IN signals, to be adjusted to have the most optimal timing. This type of tuning will allow the PLL to generate a leading skew or a lagging skew to compensate for any delay generated by the device itself and the traces. By leading skew, it indicates that the MEM_IN comes earlier than CLK_IN. Whereas by lagging skew, it indicates that the MEM_IN will come later than CLK_IN. The mechanism of generating a leading or lagging skew becomes very valuable to memory module makers since it allow the manufactures to make adjustments to the timing in order to meet any system timing requirements.

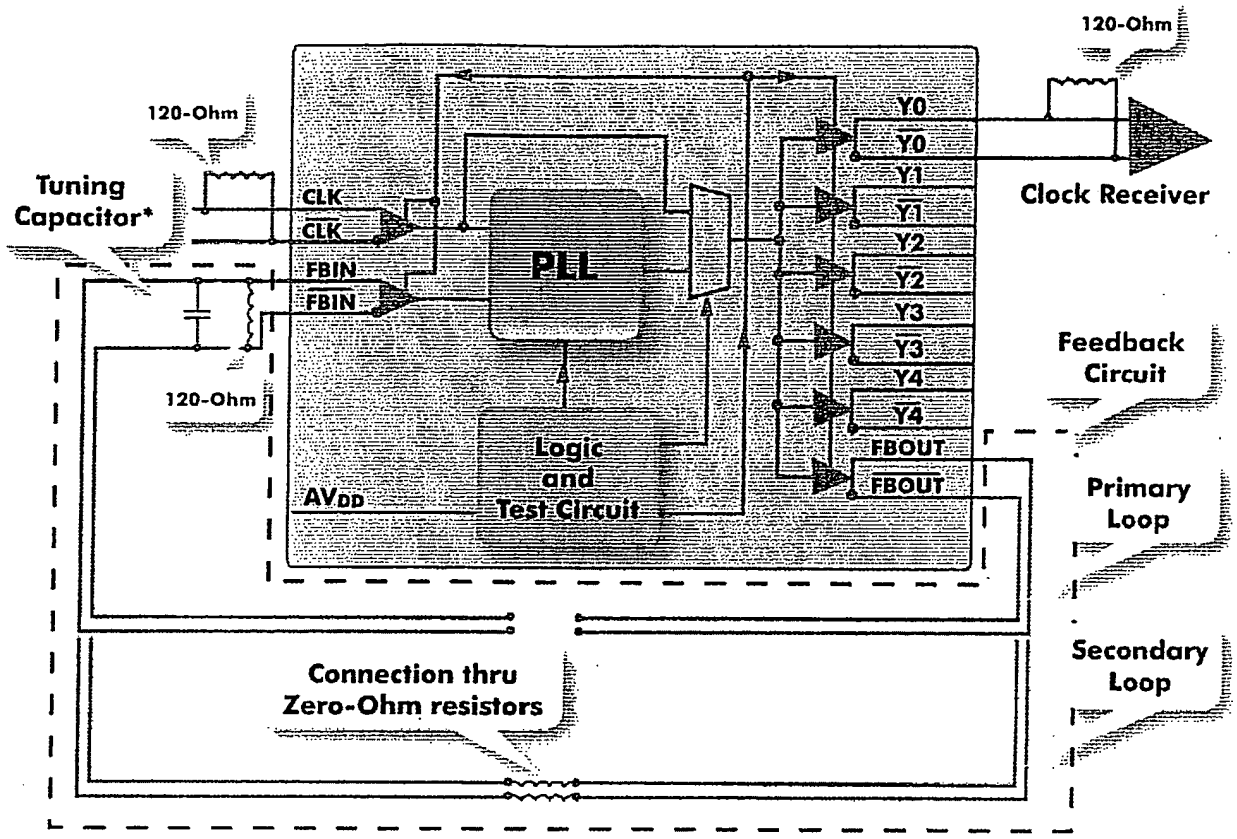
Feedback Circuit

The timing adjustment is done through the feedback loop of the PLL. The feedback circuit of the PLL is the trace and the circuit between the FBIN and FBOUT of the PLL as shown Figure 5. It is recommended that 70% to 85% of the feedback delay should be generated by the trace in the feedback loop. Note that generating more delay will cause the MEM_IN signal to lead CLK_IN. In most cases, due the constraint of board space, only one feedback loop is possible. But with components constantly reducing in size and depending on the board design, it is possible to make a secondary feedback loop. The secondary feedback loop is to provide more accessibility for adjustments once the modules have been fabricated. In situations where the module has been fabricated and the first loop does not provide any suitable timing for the system, it is still feasible to make further adjustments by disengaging the primary trace loop and connecting the secondary trace. The secondary loop can be connected through a zero-ohm resistor as shown in Figure 6. While the feedback trace will generate about 70% to 85% of the delay, the smaller delay is generated through the capacitor. The capacitor should generate a timing delay of no more than 15% to 30% since its purpose is used only to fine tune the timing. The default capacitor value is typically 0pF, but can be increased to 10pF for timing adjustments. It is strongly recommended that the capacitor value should not be too large since it can result in the feedback signal to have smaller swing range and the reduction in the slew rate leading to additional jitter. If the feedback signal has a significant amount of jitter, it will reflect to the output signals thus resulting in the degrading of the DIMMs performance. One important note to take into consideration is that it is always easier to generate delay to have MEM_IN leading CLK_IN once the board has been fabricated. However, if the system requires MEM_IN to lag CLK_IN, it is much more difficult to reduce the delay than to increase the delay since it would require the trace length to be reduced resulting in a re-spin of the board.



*Note: Tuning capacitor will vary from one system to another

Figure 5. PLL architecture and Feedback circuit



*Note: Tuning capacitor will vary from one system to another

Figure 6. Optional design with PLL secondary feedback loop

An actual application is shown graphically in Figure 7 and 8. In Figure 7, the PLL is set to have a default skew of 0ps between the input clock CLK_IN and the output clock at the memory chip MEM_IN, for simplicity. As we decreased the delay in the feedback loop by reducing the capacitor value, the skew between CLK_IN and MEM_IN becomes a lagging skew (MEM_IN comes later then CLK_IN); Figure 8a. Similarly, to generate a leading skew, MEM_IN ahead of CLK_IN, we increased the capacitor value; Figure 8b. Note that the changes are in a few hundred picoseconds. As mentioned earlier, the capacitor is mainly used to fine-tune the timing between CLK_IN and MEM_IN.

Table 3. Timing adjustment methodologies		
Skew	**Method**	**Figure**
MEM_IN Lagging CLK_IN	Decrease the delay in the feedback loop 1. Decrease the feedback capacitor in the FB loop 2. Decrease the FB loop trace length	Figure 8a
MEM_IN Leading CLK_IN	Increase the delay in the feedback loop 1. Increase the feedback capacitor in the FB loop 2. Increase the FB loop trace length	Figure 8b

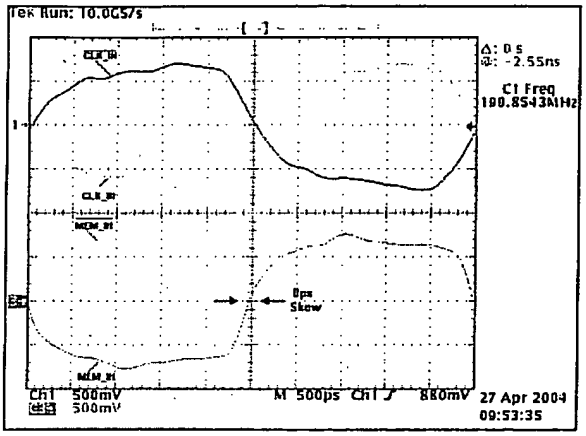


Figure 7. Skew tuned to have 0ps as reference

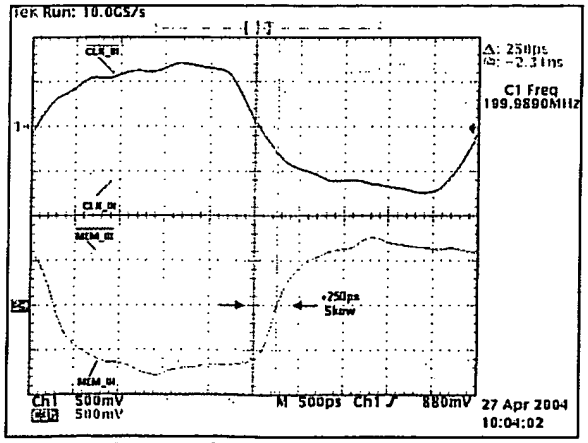


Figure 8a. Reducing the FB capacitor value will generate a lagging skew

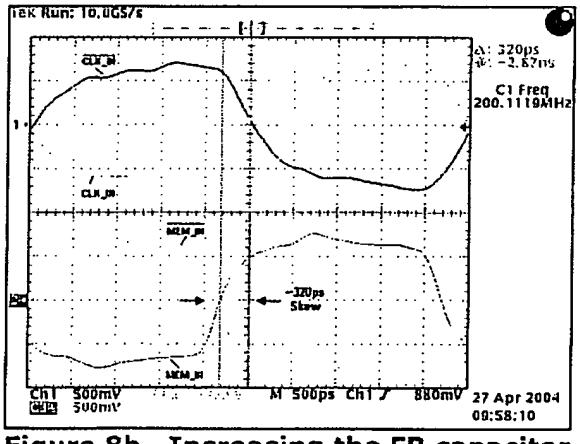
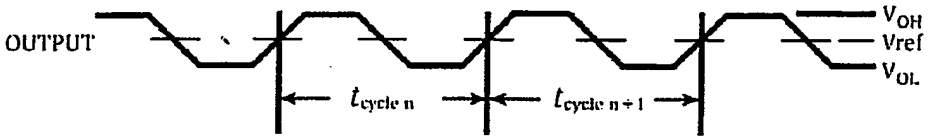


Figure 8b. Increasing the FB capacitor value will generate a leading skew

Jitter: What types are there, and how do they affect the system timing?

Since timing is extremely stringent in DDR2, jitter becomes a great concern. The PLL itself will generate some form of jitter. This is just the nature of a PLL. Even the most minute amount of jitter will eat up the system timing and can lead systematic problems. The question to address for system designers might be *what are the major types of jitter to be concerned with and how much the system can tolerate it.* Some of the major jitter parameters to take into consideration when designing with registered DIMM using PLL are addressed below:

Cycle-to-cycle jitter: The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs.



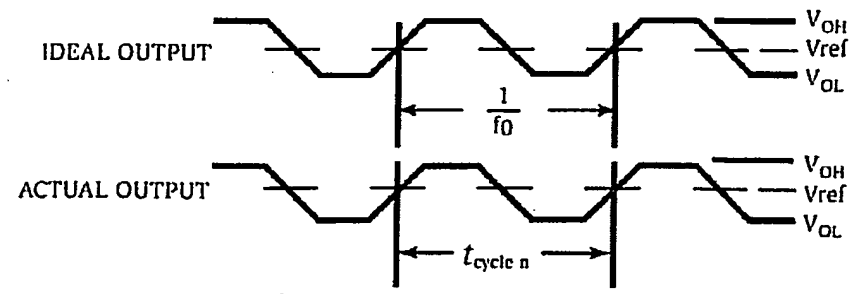
$t_{jit(cc)} = |t_{cycle\ n} - t_{cycle\ n+1}|$ where $t_{cycle\ n}$ and $t_{cycle\ n+1}$ are any two adjacent cycles measured on controlled edges.

$t_{jit(cc+)} = t_{cycle\ n+1} - t_{cycle\ n}$ where $t_{cycle\ n}$ and $t_{cycle\ n+1}$ are any two adjacent cycles measured on controlled edges, and the period of $t_{cycle\ n+1}$ is no longer than or equal to the period of $t_{cycle\ n}$.

$t_{jit(cc-)} = t_{cycle\ n} - t_{cycle\ n+1}$ where $t_{cycle\ n}$ and $t_{cycle\ n+1}$ are any two adjacent cycles measured on controlled edges, and the period of $t_{cycle\ n}$ is no longer than or equal to the period of $t_{cycle\ n+1}$.

Examples of an output waveform and cycle-to-cycle period jitter measurements

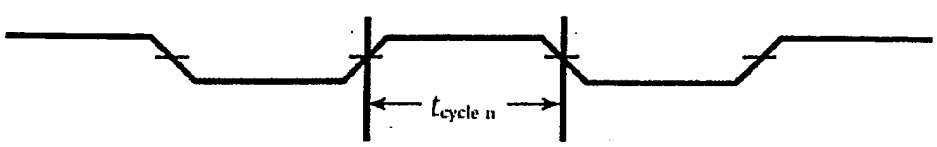
Period Jitter: The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles.



$t_{jit(per)} = t_{cycle\ n} - t_{cycle} - \frac{1}{f0}$ where $f0$ is the nominal output frequency and $t_{cycle\ n}$ is any cycle within the sample measured on controlled edges.

Example of an output waveform and jitter measurements

Half Period Jitter: The magnitude of the deviation in time duration between half cycle threshold crossing of a signal over a random sample of half cycles.



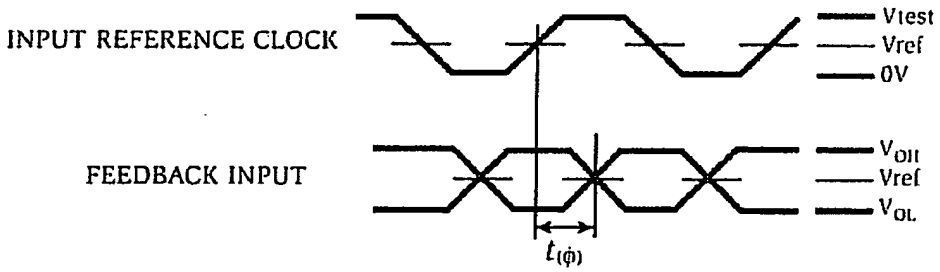
$t_{jit(hper)} = t_{hp(m)} - \frac{1}{2 \cdot f_0}$ where $f_{hp(m)}$ is the duration of any half cycle within the sample

Example of half period jitter

Peak-to-peak Jitter: The sum of cycle-to-cycle jitter, half-period jitter, and period jitter

Dynamic Phase Offset: The incremental phase offset between the input reference clock and the feedback input signal of a PLL resulting from modulations of the input reference clock.

Static Phase Offset: The time interval between similar points on the waveform of the averaged input reference clock and the averaged feedback input signal when the PLL is locked and the input reference frequency is stabled.



NOTE 1 PLL jitter may cause excursions of $t_{(\phi)}$ beyond the specified maximum.

NOTE 2 The term "PLL reference zero delay" has been used for this concept but its use is deprecated.

Example of input waveforms

To maintain the system-timing requirement, the JEDEC committee has put stringent requirements on the jitter spec.

Table 4: Jitter Specification defined by JEDEC

	DDR1 333		DDR1 400		DDR2 400		unit
	min	max	min	max	min	max	
Cycle-to-cycle Jitter	-75	+75	-40	+40	-40	+40	ps
Period Jitter	-75	+75	-40	+40	-40	+40	ps
Half-Period Jitter	-100	+100	-75	-75	-75	-75	ps

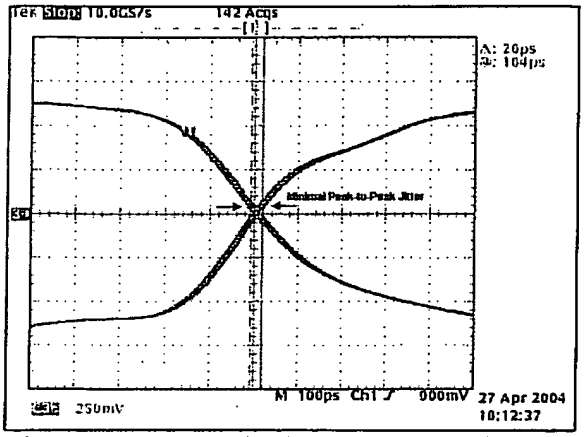


Figure 9a. PLL clock buffer with low peak-to-peak jitter

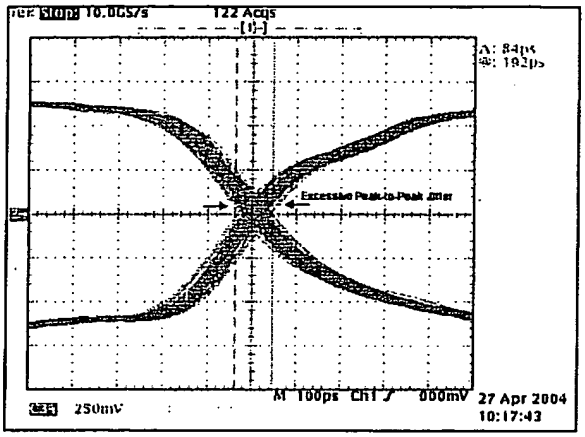


Figure 9b. PLL clock buffer with high peak-to-peak jitter

Conclusion: Market Trend

DDR1 has gained credibility for its key innovative performance while being cost effective in all market sectors. DDR2, is the next generation of memory and will continue the journey where DDR1 has left off. The market trend for DDR technology as shown is Figure 10 shows no sign of dying out. Intel, who was a supporter of Rambus, is also hopping onto the DDR bandwagon as is everyone else with chipsets such as the Grantsdale, Alderwoods, and Alviso to support both DDR1 and DDR2. As the trend in DDR technology continues to grow, Pericom Semiconductor will also grow its product line to support the memory technology. See Table 4.

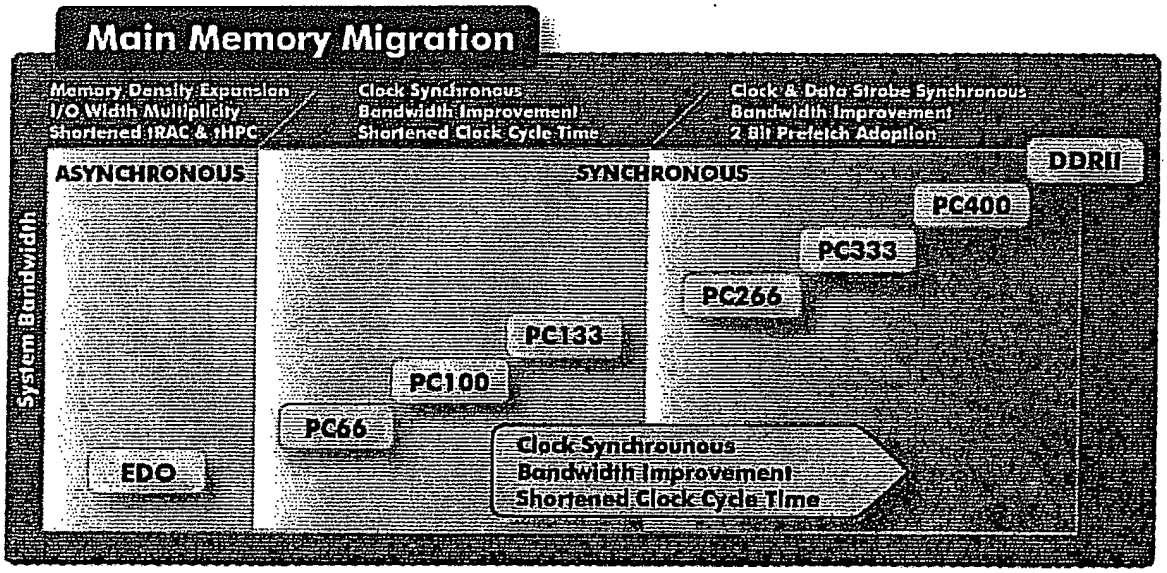


Figure 10. Architecture structure of a registered DIMM

DDR 1

PC1600 / PC2100

DIMM Configuration		Planar 9 to 18 loads	Stacked 36 Loads
Standard 1.7" DIMM	PLL	PI6CV857L	PI6CV857
	Register	PI74SSTV16857	PI74SSTV16859
1U Low Profile <1.2" DIMM	PLL	PI6CV857L	PI6CV857
	Register	PI74SSTV16857	PI74SSTV16859 PI74SSTV32852

PC2700

DIMM Configuration		Planar 9 to 18 loads	Stacked 36 Loads
Standard 1.7" DIMM	PLL	PI6CV857B	PI6CV857B
	Register	PI74SSTVF16857	PI74SSTVF16859
1U Low Profile <1.2" DIMM	PLL	PI6CV857B	PI6CV857B
	Register	PI74SSTVF16857	PI74SSTVF16859 PI74SSTVF32852

PC3200

DIMM Configuration		Planar 9 to 18 loads	Stacked 36 Loads
1U Low Profile <1.2" DIMM	PLL	PI6CVF857	---
	Register	PI74SSTVF16857A PI74SSTVF16859 PI74SSTVF16859A PI74SSTVF32852 PI74SSTVF32852A	---

DDR 2

PC2-3200 / PC2-4300

DIMM Configuration		Planar 9 to 18 loads	Stacked 36 Loads
1U Low Profile <1.2" DIMM	PLL	PI6CU877	---
	Register	PI74SSTU32864 PI74SSTU32864A PI74SSTU32866	---

SDR

PC100 / PC133

DIMM Configuration	PC100 / PC133	
	Planar	Stacked
Frequency	100MHz / 133MHz	100MHz / 133MHz
PLL Clock	PI6C2510-133E	PI6C2510-133E
Registered Buffer	PI74ALVC162834F	PI74AVC+16334
Registered Buffer	PI74ALVC162835F	PI74AVC+16836
Registered Buffer	-	PI74AVC16834
Registered Buffer	-	PI74AVC16835

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Revision of JESD65-A
September 2003

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